Code No: 153AB **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, February - 2024
ANALOG AND DIGITAL ELECTRONICS
(Common to CSE, IT, ECM, ITE, CE(SE), CSE(CS), CSE(N))

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A
(25 Marks)

1.a)	Draw the electrical equivalent model of a diode and identify elements.	[2]
b)	Define clipping and clamping circuits.	[3]
c)	Mention the applications of Transistors.	[2]
d)	List out the different types of biasing methods and stability factors.	[3]
e)	Define Pinch off Voltage.	[2]
f)	Compare between TTL gate, RTL gate and DCTL gates.	[3]
g)	State distributive laws with examples.	[2]
h)	What are minterms and maxterms? Give examples for each.	[3]
i)	Draw the state table and excitation table of the T flip flop.	[2]
j)	What is state assignment? Give one example.	[3]

PART – B
(50 Marks)

2.a) Draw and explain the V-I characteristics of a tunnel diode.
b) Draw the circuit diagram of the half-wave rectifier and explain its operation with the help of waveforms. [5+5]

OR

3.a) Derive the expression for ripple for the circuit FWR with an inductor filter.
b) How does the reverse saturation current of a diode vary with temperature? Explain. [5+5]

4.a) Compare CB, CE and CC configurations of BJT.
b) Explain various methods used for coupling of multistage amplifiers with their frequency response. [5+5]

OR

5.a) With a neat diagram explain the input, output and current gain characteristics of a transistor in CC configuration.
b) Explain how the transistor acts as an amplifier. [5+5]

6.a) Explain ECL gate and write the advantages and disadvantages.
b) With a neat sketch explain the characteristics of P-channel JFET. [5+5]

OR

7.a) Draw and explain the CS amplifier with current source load.

b) Explain the operation of the DTL NAND gate with a neat diagram. [5+5]

8.a) Draw and explain the 1 bit magnitude Comparator.

b) Design the full adder by using logic gates and write suitable equations. [5+5]

OR

9.a) Explain in detail about Binary Multiplier.

b) Simplify the following function using K-map. $F(A,B,C,D) = \Sigma(1,3,4,5,6,11,13,14,15)$. [5+5]

10.a) Design a modulo 10 counter using JK flipflops and explain its timing diagram.

b) Differentiate between Latch and flip flop with suitable examples. [6+4]

OR

11.a) Compare and contrast static RAM and dynamic RAM.

b) Explain about Ring counter with suitable diagrams. [5+5]

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